JEDEC STANDARD

Thermal Impedance Measurement for Insulated Gate Bipolar Transistors – (Delta $V_{CE(on)}$ Method)

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THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS - (DELTA $V_{CE(on)}$ METHOD)

(From JEDEC board Ballot JCB-04-38, formulated under the cognizance of the JC-25 Committee on Transistors.)

1 Scope

The purpose of this test method is to measure the thermal impedance of the IGBT (Insulated Gate Bipolar Transistor) under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the collector-emitter on voltage, $V_{CE(on)}$, is used as the junction temperature indicator. This is an alternative method to JEDEC Standard No. 24-6.

2 Terms and definitions

The following symbols and terms shall apply for the purpose of this test method:

I_M Emitter current applied during measurement of the collector-emitter ON voltage.

I_H Heating current through the collector or the emitter lead.

V_H Heating voltage between the collector and emitter.

P_H Magnitude of the heating power pulse applied to the DUT in watts(W); the product of I_H and V_H.

t_H Heating time during which P_H is applied.

$\alpha_{VCE(on)}$ Voltage-temperature coefficient of $V_{CE(on)}$ with respect to T_J; in mV/°C.

K Thermal calibration factor equal to the reciprocal of $\alpha_{VCE(on)}$; in °C/mV.

T_J Junction temperature in degrees Celsius (°C).

T_{JI} Junction temperature in degrees Celsius (°C) before the start of the power pulse.

T_{JF} Junction temperature in degrees Celsius (°C) after the end of the power pulse.

2 Terms and definitions (cont'd)

T_X Reference temperature in degrees Celsius (°C).

T_{XI} Reference temperature in degrees Celsius (°C) before the start of the power pulse.

T_{XF} Reference temperature in degrees Celsius (°C) after the end of the power pulse.

$V_{CE(on)}$ Collector-emitter voltage in millivolts (mV).

$V_{CE(on)i}$ Collector-emitter voltage in millivolts (mV) before the start of the power pulse.

$V_{CE(on)f}$ Collector-emitter voltage in millivolts (mV) after the end of the power pulse.

$V_{CE(M)}$ Collector-emitter voltage during measurement periods.

V_{CE} Collector-emitter voltage during heating period.

V_{GE} Gate-emitter voltage used to drive the device during the heating period.

t_{MD} Measurement delay time; is defined as the time from the removal of the heating pulse, P_H, to the start of the $V_{CE(on)}$ measurement.

t_{SW} Sample window time during which the final $V_{CE(on)}$ measurement is made.

$Z_{\theta JX}$ Transient junction to reference point thermal impedance in degrees Celsius/watt(°C/W). $Z_{\theta JX}$ for a specified power pulse duration is:

$$Z_{\theta JX} = \frac{(T_{JF} - T_{JI}) - \Delta T_X}{P_H}$$

where: ΔT_X = the change in reference point temperature during the heating pulse (for short heating pulses, such as at die attach evaluations, this term becomes negligible)

$R_{\theta JX}$ the value referred to as steady state thermal resistance. This is the condition where the time of the heating pulses is sufficiently long that there is no change in the value of $Z_{\theta JX}$, or where $[(T_{JF} - T_{JI}) - \Delta T_X]$ does not change.

3 Apparatus

The apparatus for this test shall include the following:

3.1 A means for temperature measurements

The preferred method for measuring the case temperature is a thermocouple to measure a consistent reference location. The preferred reference location is on the case under the heat source, the IGBT die. The thermocouple wire should be AWG size 30; copper-constantan (type T) is preferred to optimize temperature reading response. The junction thermocouple shall be welded, not soldered or twisted, to form a bead. Proper mounting of the thermocouple to ensure intimate contact to the reference is critical for system accuracy, which shall be ±0.5 °C.
Alternative methods to measure the referenced case temperature can be used, such as IR thermal imaging, but these methods are usually less desirable economically. The method for temperature measurement is not relevant to this test method as long as the accuracy of the temperature measurement system is ±0.5 °C.

3.2 A setup for $\alpha_{VCE(on)}$ or K-factor calibration

A $\alpha_{VCE(on)}$ or K-factor calibration shall be determined using a controlled environment. A recirculating bath or an oven that is capable of holding the case temperature during the device calibration to within ±1 °C over a 25 °C to 125 °C range, the possible temperature range for measuring the K-factor, can be used. A circuit, such as Figure 1, shall be used to make the measurement to determine this K-factor. The current source used to generate I_M shall have an accuracy to ±2% . The meter used to measure $V_{CE(on)}$ shall be capable of 1 mV resolution. The V_{GE} supply shall have an accuracy to ±2%. The wires used to supply the device to current source connections shall be sufficient to handle the measurement current (AWG 22 is sufficient to carry up to 100 mA). A typical $V_{CE(on)}$ vs. Temperature curve will be similar to Figure 2.

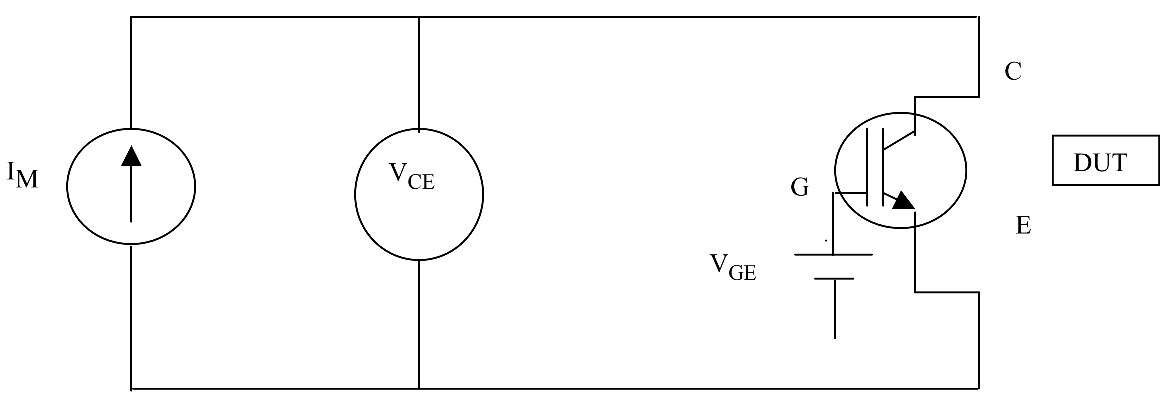


Figure 1 — Simplified schematic for Rthjc measurement

3 Apparatus (cont'd)

3.3 A setup for thermal testing

Testing can be implemented using a circuit that allows the control of the test current, I_H, and the measurement current, I_M, through the use of a high speed switching circuit. This circuit should effectively measure the $V_{CE(on)}$ at I_M during the pre-power application phase of the test. The measurement will be held for later comparison to the post power measurement. Then the circuit will switch to the high current mode and will set up the switches that control I_H and V_H during the heating phase of the thermal testing. After the heating pulse is complete the circuit should effectively measure the $V_{CE(on)}$ at I_M as done during the pre-power application.

4 Measurement of the temperature sensitive parameter

4.1 $V_{CE(on)}$ versus temperature calibration

The required calibration of $V_{CE(on)}$ vs. T_J, or $\alpha_{VCE(on)}$, is accomplished by monitoring $V_{CE(on)}$ and I_M as the heat sink temperature (and thus the DUT temperature) is varied by external heating. V_{GE} shall be set at a condition that results in the DUT being full on. I_M must be chosen so that there is no significant self-heating but provides sufficient temperature sensitivity. This will be dependent upon the DUT power dissipation, or the DUT die size (I_M could be 1 mA or less for smaller devices and upward of 100 mA for larger devices). It is prudent engineering practice to generate this curve with more then 3 points. A typical calibration curve usually has a linear relation over a 25 °C to 125 °C range, such as Figure 2.

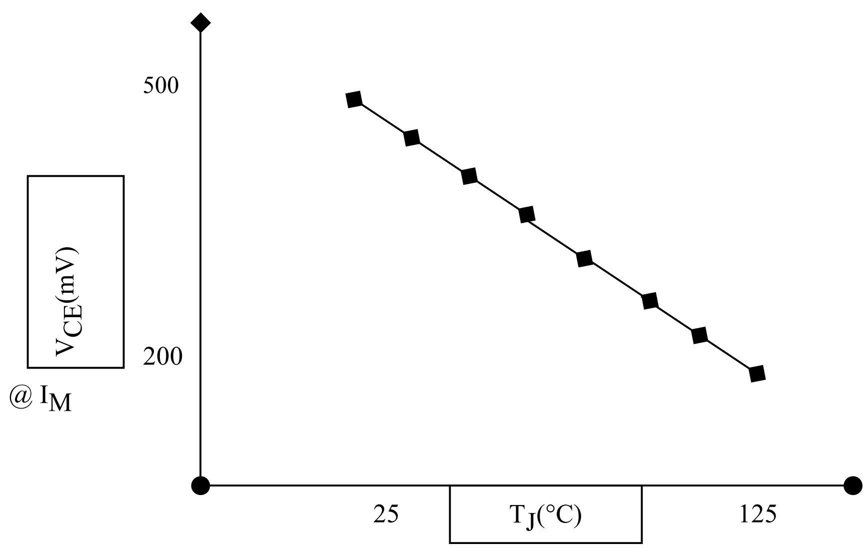


Figure 2 — Example of a calibration curve

4 Measurement of the temperature sensitive parameter (cont'd)

4.1 $V_{CE(on)}$ versus temperature calibration (cont'd)

A suitable sample-and-hold voltmeter or oscilloscope shall be used to measure the collector-emitter voltage at selected temperatures. $V_{CE(on)}$ shall be measured within ±1 mV, or within ±2% of $\Delta V_{CE(on)}$, which ever is less.

4.2 K-factor

A calibration factor, K (which is the reciprocal of the slope of the curve on Figure 2) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{CE2} - V_{CE1}} \right| \ °C/mV$$

It has been observed experimentally that the $\alpha_{VCE(on)}$ or K-factor variation for devices within a given device type class is small. This should be verified. Usually a 10 to 12 piece sample from a device lot can be measured. The average, K_{AV}, and standard deviation (σ_K), of the K-factor is determined. If σ_K is less than or equal to ±3% of K_{AV}, then K_{AV} can be used. If σ_K is greater than ±3% of K_{AV}, then all the devices in the lot need to be measured for their respective K-factor and the individual values for the $\alpha_{VCE(on)}$ shall be used for the calculations of thermal resistance or thermal response. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacturer shall use statistical techniques to establish the limits.

5 Test procedure

5.1 Calibration

K-factor determination shall be done per 4, being mindful of the constraints in 4.2.

5.2 Reference temperature point

The reference temperature point location must be specified and the temperature shall be monitored using the requirements of 3.1. The reference point is usually chosen to be on the bottom of the transistor case directly below the IGBT die. Alternatively, this reference point should be as close to the thermal path generated by the die into the case (or the heat sink location that is accessible) as practicable, so it reflects the effects of mounting the DUT in a real application.

5 Test procedure (cont'd)

5.2 Reference temperature point (cont'd)

If it is determined that the temperature T_X increases more than 5 % of the measured junction temperature rise during the power pulse, then one of following options must be taken. The heating pulse magnitude must be decreased. Or the DUT must be mounted to a temperature controlled heat sink and temperatures must be measured properly to assure the T_X requirement. Or the calculated value of thermal impedance must be corrected to take into account the thermal impedance of the reference point to the cooling medium (i.e., the heat sink).

Temperature measurements for monitoring, controlling and/or correcting for reference point temperature changes are not required if the t_H is short enough to ensure that the heat generated by the DUT has not had time to propagate through the package. In this case typical values for t_H are 10 ms to 100 ms dependent upon the package design and materials.

5.3 Steady state thermal resistance, $R_{\theta JX}$

Prior to the power pulse:

a) Establish the reference point temperature T_{XI}.
b) Apply the gate voltage, V_{GE}, needed to assure full conduction.
c) Measure the initial $V_{CE(on)i}$ at the specified I_M.

Apply the power pulse

a) Verify V_H, observe that there are no anomalies with the pulse.
b) Verify I_H, observe that there are no anomalies with the pulse.
c) Verify that t_H is great enough that the device is in a steady state condition.
d) Measure the T_{XF} at the end of the power pulse.

Post Power Pulse

a) Apply the gate voltage, V_{GE}, needed to assure full conduction.
b) Measure the $V_{CE(on)f}$ at the specified I_M.
c) Establish the delay time, t_{MD}. This can be used to extrapolate the 'actual' T_{JF} of the post power pulse.

5 Test procedure (cont'd)

5.4 Thermal response, $Z_{\theta JX}$

Prior to the power pulse:

a) Establish the reference point temperature T_{XI}.

b) Apply the gate voltage, V_{GE}, needed to assure full conduction.

c) Measure the initial $V_{CE(on)i}$ at the specified I_M.

Apply the power pulse

a) Verify V_H, observe that there are no anomalies with the pulse.

b) Verify I_H, observe that there are no anomalies with the pulse.

c) Verify that t_H is short enough that the device is not exceeding the conditions of paragraph 5.2 for a non-heat-sunk device. This can be done by measuring the T_{XF} at the end of the power pulse.

Post Power Pulse

a) Apply the gate voltage, V_{GE}, needed to assure full conduction.

b) Measure the $V_{CE(on)f}$ at the specified I_M.

c) Establish the delay time, t_{MD}. This can be used to extrapolate the 'actual' T_{JF} of the post power pulse.

5.5 Calculate thermal resistance, $R_{\theta JX}$, or thermal impedance, $Z_{\theta JX}$

a) The value of thermal resistance is calculated per the formula below:

$$R_{\theta JX} = \{\Delta T_J / P_H\} - \{\Delta T_X / P_H\}$$
$$= [(\{ V_{CE(on)f} - V_{CE(on)I} \} / \alpha_{VCE(on)}) / P_H] - \{\Delta T_X / P_H\} \quad °C/W$$

b) The value of thermal response is calculated per the formula below:

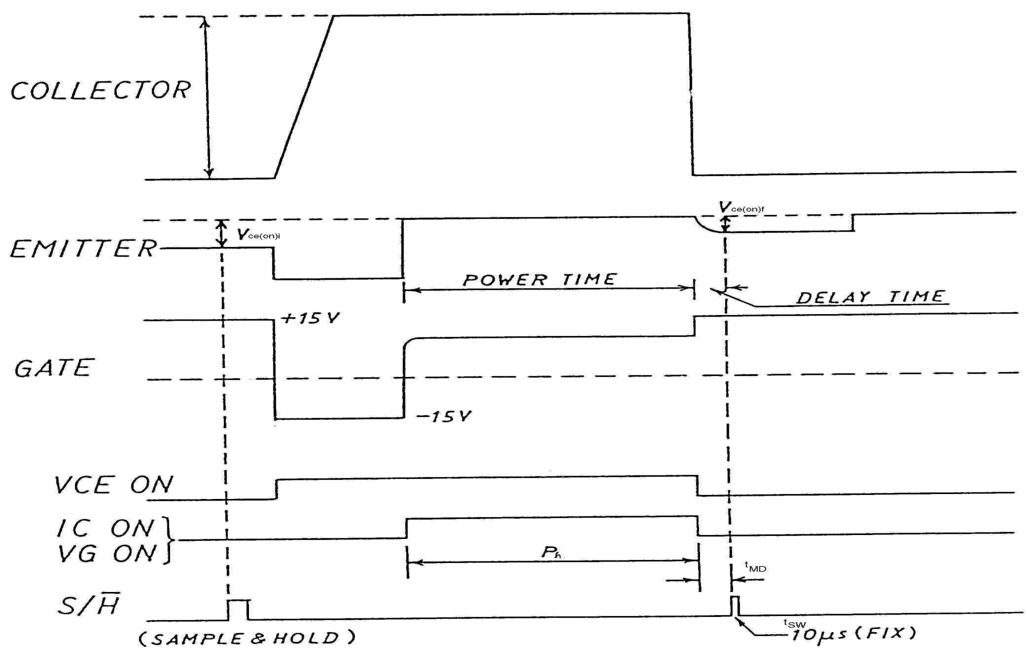
$$Z_{\theta JX} = \{\Delta T_J / P_H\}$$
$$= (\{ V_{CE(on)f} - V_{CE(on)I} \} / \alpha_{VCE(on)}) / P_H \quad °C/W$$

because the term $\{\Delta T_X / P_H\}$ approaches 0 if the conditions for thermal response are met.

NOTE There are several semi-automated systems available today, because of the advances made in computer controlled testing systems, that can do much of the data taking and calculations for the procedures outlined in this section.

6 Test conditions and measurements

Typical waveforms are below



where VCE1 = $V_{CE(on)i}$

VCE2 = $V_{CE(on)f}$

DT = Delay time = t_{MD}

PT = P_H [t_{SW} = the sampling window, (10 µs) this value is not always fixed]

NOTE 1 Some test equipment may provide a ΔV_{CE} directly instead of $V_{CE(on)i}$ and $V_{CE(on)f}$; this is an acceptable alternative. Record the value of ΔV_{CE}.

NOTE 2 Some test equipment may provide $Z_{\theta JX}$ directly instead of $V_{CE(on)i}$ and $V_{CE(on)f}$ for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

NOTE 3 Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used.

7 Test conditions and measurements to be specified and recorded

7.1 K factor calibration

7.1.1 <u>Test conditions,</u> Specify the following test conditions:

a) I_M measuring current ___ mA
b) Initial junction temperature ___ °C
c) Initial V_{CE} voltage ___ mV
d) Final junction temperature ___ °C
e) Final V_{CE} voltage ___ mV

7.1.2 <u>K factor,</u> Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{CE2} - V_{CE1}} \right| \ °C/mV$$

K factor ___ °C/mV

7.2 Thermal transient and equilibrium measurements

7.2.1 <u>Test conditions,</u> Specify the following test conditions:

a) I_M measuring current ___ mA
b) I_H heating current ___ A
c) V_H heating voltage ___ V
d) t_H heating time ___ ms
e) t_{MD} measurement time delay ___ µs
f) t_{SW} sample window time ___ µs

7.2.2 <u>Data,</u> Record the following data:

a) $V_{CE(on)i}$ initial forward voltage ___ V
b) $V_{CE(on)f}$ final forward voltage ___ V

NOTE 1 Some test equipment may provide a ΔV_{CE} instead of $V_{CE(on)i}$ and $V_{CE(on)f}$; this is an acceptable alternative. Record the value of ΔV_{CE}.

NOTE 2 Some test equipment may provide direct display of calculated $Z_{\theta JX}$; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.)

Standard Improvement Form **JEDEC JESD24-12**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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   - [ ] Test method number ___________ Clause number ___________

   The referenced clause number has proven to be:
   - [ ] Unclear [ ] Too Rigid [ ] In Error
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2. Recommendations for correction:

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3. Other suggestions for document improvement:

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